CLIPPEDIMAGE= JP354158826A
PAT-NO: JP354158826A
DOCUMENT-IDENTIFIER: JP 54158826 A
TITLE: DATA MEMORY SYSTEM

PUBN-DATE: December 15, 1979

INVENTOR-INFORMATION:
NAME
YAMAZAKI, KIYOHIRO
NAKAMURA, SHIGERU
TANIGUCHI, TORU
KURATA, MASAAKI
TOMIZAWA, SHINICHI

ASSIGNEE-INFORMATION:
NAME COUNTRY
FUJITSU LTD N/A

APPL-NO: JP53067982
APPL-DATE: June 5, 1978

INT-CL_(IPC): G11C007/00; G06F013/00 ; G11C008/00
US-CL-CURRENT: 365/230.01

ABSTRACT:
PURPOSE: To make it possible to perform processes in a first-in first-out mode
by storing input data in an input order, by reading and outputting them in the
input order and also by clearing the memory equivalently after all stored data
are outputted.

CONSTITUTION: When the time needed for data processing is longer than that for data inputting and input data are received one after another during the data processing, write address counter WAC1 advances by clock CLW at every time when data are inputted and the input data are written sequentially at addressed assigned by WAC1. At this time, the data processing progresses without influencing the write of the input data to read-write memory MEM5. Next, read address 2 increases at every time when the process of the output data ends, and consequently data stored 5 are read out in the opposite order of the read, stored in output register 6 sequentially, and outputted 8 by clock CLD at every time when the process of preceding data ends. Namely, circuit 10 serves as a first-in first-out circuit.

CLIPPEDIMAGE= JP358063283A
PAT-NO: JP358063283A
DOCUMENT-IDENTIFIER: JP 58063283 A
TITLE: ORDER CONVERTING CIRCUIT

PUBN-DATE: April 15, 1983

INVENTOR-INFORMATION:
NAME
FUKUI, AKIRA
KIKUCHI, SHIRO
KAWAGUCHI, MASAHARU
MORI, MAKOTO
OSAKI, TAKAAKI

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NEC CORP	N/A
NIPPON TELEGR & TELEPH CORP <NTT>	N/A
OKI ELECTRIC IND CO LTD	N/A
HITACHI LTD	N/A
FUJITSU LTD	N/A

APPL-NO: JP56161963
APPL-DATE: October 13, 1981

INT-CL_(IPC): H04Q001/45
US-CL-CURRENT: 365/230.09

ABSTRACT:
PURPOSE: To eliminate a selector, by storing the writing and reading addresses into an address control memory so as to read the information out

of a buffer memory in the order different from the order by which the information is written into the buffer memory.

CONSTITUTION: The output of a control counter 5 is fed to an address control memory 6, and the output of the memory 6 is supplied to a buffer memory 4 which stores temporarily the input signal in the form of the address of the memory 4. The output of the memory 4 is turned into an output signal 11 with the converted order. Both writing and reading addresses of the memory 4 are written into the memory 6 in the case of the random writing and sequential reading and vice versa. As a result, the memory 6 can read out the information in the order different from the order by which the information is written into the memory 4.